Docket No.: 22270-00001-US1

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

- (Original) A clock multiplier, comprising: 1.
- a first clock multiplication circuit for multiplying the frequency of an input clock based on a delay time;
 - an inverter for inverting the output clock of the first clock multiplication circuit;
 - a first low pass filter connected to the output of the inverter;
- a second low pass filter connected to the output of the first clock multiplication circuit; and
- an amplifier for comparing the output voltages of the first low pass filter and the second low pass filter so as to feedback-control the delay time of the first clock multiplication circuit.
- (Original) The clock multiplier in accordance with Claim 1, wherein the first 2. clock multiplication circuit comprises:
- a first voltage-controlled delay line for delaying the input clock by the delay time; and
- a first exclusive OR (XOR) gate connected to the input clock and the output of the first voltage-controlled delay line.
- 3. (Original) The clock multiplier in accordance with Claim 2, wherein the first voltage-controlled delay line is operative to delay the input clock by one-fourth period of the input clock.

P.03/07

Application No.: 10/649,706

Docket No.: 22270-00001-US1

4. (Original) The clock multiplier in accordance with Claim 2, which is a clock doubler.

- 5. (Original) The clock multiplier in accordance with Claim 1, wherein the duty cycle of the output clock of the first clock multiplication circuit is approximately 50%.
- 6. (Original) The clock multiplier in accordance with Claim 1, wherein the first clock multiplication circuit comprises:

a first voltage-controlled delay line for delaying the input clock by the delay time;

an XOR gate connected to the input clock and the output of the first voltagecontrolled delay line;

a second voltage-controlled delay line for delaying the output clock of the first voltage-controlled delay line by the delay time; and

an exclusive NOR (XNOR) gate connected to the outputs of the XOR gate and the second voltage-controlled delay line.

- 7. (Original) The clock multiplier in accordance with Claim 6, wherein the first voltage-controlled delay line and the second voltage-controlled delay line respectively delay the input clock and the output clock of the first voltage-controlled delay line by one-sixth period of the input clock.
- 8. (Original) The clock multiplier in accordance with Claim 6, which is a 3X clock multiplier.
- 9. (Original) The clock multiplier in accordance with Claim 2, further comprising a second clock multiplication circuit, which comprises:

a second voltage-controlled delay line for delaying the output of the first XOR gate by the delay time; and

Docket No.: 22270-00001-US1

a second XOR gate connected to the outputs of the first XOR gate and the second voltage-controlled delay line.

- 10. (Original) The clock multiplier in accordance with Claim 9, wherein the first voltage-controlled delay line and the second voltage-controlled delay line respectively delay the input clock and the output clock of the first XOR gate by one-fourth period and one-eighth period of the input clock.
- 11. (Original) The clock multiplier in accordance with Claim 9, which is a 4X clock multiplier.
- 12. (Original) The clock multiplier in accordance with Claim 10, wherein the first voltage-controlled delay line is constituted by a third voltage-controlled delay line and a fourth voltage-controlled delay line connected in series, and the third voltage-controlled delay line and the fourth voltage-controlled delay line individually delay the input clock by one-eighth period of the input clock.
 - 13. (Currently amended) A clock multiplier, comprising:

a first clock multiplication circuit for multiplying the frequency of an input clock based on a delay time;

a second low pass filter connected to the output of the first clock multiplication circuit;

an amplifier for comparing a one-half supply voltage and the output voltage of the second low pass filter so as to feedback-control the delay time of the first clock multiplication circuit; and

a second clock multiplication circuit, which comprises:

a second voltage-controlled delay line for delaying the output of-the-a first XOR gate by the delay time; and

Docket No.: 22270-00001-US1

a second XOR gate connected to the outputs of the first XOR gate and the second voltage-controlled delay line.

- (Currently amended) The clock multiplier in accordance with Claim 13, wherein 14. the first clock multiplication circuit comprises:
- a first voltage-controlled delay line for delaying the input clock by the delay time; and,
- a-wherein the first XOR gate is connected to the input clock and the output of the first voltage-controlled delay line.
- 15. (Original) The clock multiplier in accordance with Claim 13, wherein the duty cycle of the output clock of the first clock multiplication circuit is approximately 50%.
 - 16. (Previously presented) A clock multiplier, comprising:
- a first clock multiplication circuit for multiplying the frequency of an input clock based on a delay time;
- a second low pass filter connected to the output of the first clock multiplication circuit; and
- an amplifier for comparing a one-half supply voltage and the output voltage of the second low pass filter so as to feedback-control the delay time of the first clock multiplication circuit,

wherein the first clock multiplication circuit comprises:

- a first voltage-controlled delay line for delaying the input clock by the delay time;
- an XOR gate connected to the input clock and the output of the first voltagecontrolled delay line;

Docket No.: 22270-00001-US1

a second voltage-controlled delay line for delaying the output of the first voltagecontrolled delay line by the delay time; and

an XNOR gate connected to the outputs of the XOR gate and the second voltagecontrolled delay line.

Claim 17: (Canceled)

(Previously presented) The clock multiplier in accordance with Claim 16, 18. wherein the duty cycle of the output clock of the first clock multiplication circuit is approximately 50%.